WHAT IS CLAIMED IS:

1. (Currently amended) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate;

a data wire formed on the insulating substrate and intersecting the gate wire in an insulating manner;

a thin film transistor electrically connected to the gate wire and the data wire;

a direction control electrode electrically connected to a terminal of the thin film transistor; ~~and~~

a pixel electrode electrically insulated from the direction control electrode and having a cutout, wherein the cutout substantially coinciding with the configuration of the direction control electrode; and

a metallic piece formed of the same layer as the gate wire and placed under the direction control electrode, wherein the metallic piece substantially coincides with the configuration of the direction control electrode.

2. (Original) The thin film transistor array panel of claim 1, further comprising a storage electrode wire intersecting the data wire and forming a storage capacitor in association with the pixel electrode.

3. (Currently amended) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate and including a gate electrode and a gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire including a data line formed on the semiconductor layer and intersecting the gate line, a source electrode connected to the data line, and a drain electrode facing the source electrode;

a direction control electrode connected to the drain electrode;

a passivation layer formed on the data wire and the direction control electrode; and

a pixel electrode formed on the passivation layer with a cutout , the cutout substantially coinciding with the configuration of the direction control electrode,

wherein the semiconductor layer comprises a direction control electrode semiconductor located under the direction control electrode along the direction control electrode.

4. (Original) The thin film transistor array panel of claim 3, further comprising:

a gate pad connected to one end of the gate line;

a data pad connected to one end of the data line;

a subsidiary gate pad formed on the passivation layer and connected to the gate pad through a contact hole; and

a subsidiary data pad formed on the passivation layer and connected to the data pad through a contact hole.

5. (Original) The thin film transistor array panel of claim 3, wherein the cutout of the pixel electrode includes a plurality of X-shaped portions and a plurality of rectilinear portions, and the direction control electrode overlaps the X-shaped portions.

6. (Currently amended) The thin film transistor array panel of claim 3, wherein the semiconductor layer further comprises a data-line semiconductor located under the data line and a channel semiconductor located under the source and the drain electrodes.

7. (Canceled)

8. (Original) The thin film transistor array panel of claim 3, further comprising a metallic piece formed of the same layer as the gate wire and placed under the direction control electrode along the direction control electrode.

9. (Currently amended) A liquid crystal display comprising:

a first insulating substrate;

a gate wire formed on the first insulating substrate;

a data wire formed on the first insulating substrate and intersecting the gate wire in an insulating manner to define a pixel area;

a direction control electrode formed in the pixel area defined by the intersection of the gate wire and the data wire;

a thin film transistor connected to the gate wire, the data wire, and the direction control electrode;

an electrically floating pixel electrode formed in the pixel area, electrically insulated from the direction control electrode connected to the thin film transistor, and having a cutout substantially coinciding with the configuration of the direction control electrode;

a second insulating substrate facing the first insulating substrate;

a common electrode formed on the second insulating substrate; ~~and~~

a liquid crystal layer interposed between the first substrate and the second insulating substrate; and

a metallic piece formed of the same layer as the gate wire and placed under the direction control electrode, wherein the metallic piece substantially coincides with the configuration of the direction control electrode.

10. (Original) The liquid crystal display of claim 9, wherein the liquid crystal layer has negative dielectric anisotropy and liquid crystal molecules in the liquid crystal layer are aligned perpendicular to the first and the second substrates.

11. (Original) The liquid crystal display of claim 9, wherein the liquid crystal layer has positive dielectric anisotropy and liquid crystal molecules in the liquid crystal layer are aligned parallel to the first and the second substrates.

12. (Original) The liquid crystal display of claim 9, further comprising a storage electrode wire formed on the first substrate and forming a storage capacitor in association with the pixel electrode.

13. (Original) The liquid crystal display of claim 12, wherein the common electrode and the storage electrode wire are supplied with the same voltage, and voltage difference between the

pixel electrode and the common electrode V_{PC} is given by:

$$V_{PC} = [(C_{DP}) / (C_{DP} + C_{LC} + C_{ST})] \times V_{DC},$$

where C_{DP} indicates capacitance between the direction control electrode and the pixel electrode, C_{LC} indicates capacitance between the pixel electrode and the common electrode, C_{ST} indicates capacitance between the pixel electrode and the storage electrode wire, and V_{DC} is the voltage difference between the direction control electrode and the common electrode.

14. (New) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate and including a gate electrode and a gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire including a data line formed on the semiconductor layer and intersecting the gate line, a source electrode connected to the data line, and a drain electrode facing the source electrode;

a direction control electrode connected to the drain electrode;

a passivation layer formed on the data wire and the direction control electrode; and

a pixel electrode formed on the passivation layer with a cutout , the cutout substantially coinciding with the configuration of the direction control electrode,

wherein the semiconductor layer comprises a data-line semiconductor located under the data line and a channel semiconductor located under the source and the drain electrodes.